

12/19/00

JC944 U.S. PTO

Express Mail Label No.: EL443496588US

PATENT

Case Docket No.: 00P9102US

Date: December 19, 2000

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231
Box PATENT APPLICATION

Sir:

Transmitted herewith for filing is the patent
application of:

Inventor(s): Mihel Seitz, Michael L. Wise and Christian Dubuc

For: **Method For Fabricating Transistors Having Damascene Formed
Gate Contacts And Self-Aligned Borderless Bit Line Contacts**

This application includes:

20 pages: specification, claims and abstract
16 sheets of formal drawings
photographs

Also enclosed is:

Declaration and Power of Attorney
Information Disclosure Statement pursuant to 37 CFR 1.56.

The filing fee has been calculated as shown below:

FOR:	(Col. 1) NO. FILED	(Col. 2) NO. EXTRA FEE	OTHER THAN A SMALL ENTITY FEE
BASIC FEE	XXXXXXXX	XXXXXXXXXX	XXXXX \$710.
TOTAL CLAIMS	18 - 20 =		x 18. = \$
INDEP CLAIMS	5 - 3 =	2	x 80. = \$160.
* MULTIPLE DEPENDENT CLAIM PRESENTED			+270. = \$
TOTAL			\$870.

- ☒ Please charge my Deposit Account No. 19-2179 in the amount of \$870.00. A duplicate copy of this sheet is enclosed.
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- ☒ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

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APPLICATION FOR LETTERS PATENT
OF THE UNITED STATES

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TITLE OF INVENTION:

METHOD FOR FABRICATING
TRANSISTORS HAVING DAMASCENE
FORMED GATE CONTACTS AND SELF-
ALIGNED BORDERLESS BIT LINE
CONTACTS

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION